

Thermodynamic and kinetic control of the lateral Si wire growth

Sergey N. Dedyulin^{a)} and Lyudmila V. Goncharova

Department of Physics and Astronomy, The University of Western Ontario, 1151 Richmond St., London, Ontario N6A 3K7, Canada

(Received 27 December 2013; accepted 11 March 2014; published online 25 March 2014)

Reproducible lateral Si wire growth has been realized on the Si (100) surface. In this paper, we present experimental evidence showing the unique role that carbon plays in initiating lateral growth of Si wires on a Si (100) substrate. Once initiated in the presence of \approx 5 ML of C, lateral growth can be achieved in the range of temperatures, T = 450–650 °C, and further controlled by the interplay of the flux of incoming Si atoms with the size and areal density of Au droplets. Critical thermodynamic and kinetic aspects of the growth are discussed in detail. © 2014 AIP Publishing LLC. [http://dx.doi.org/10.1063/1.4869444]

The vapour-liquid-solid (VLS) model was first proposed in the early 1960s,¹ and it remains the most utilized paradigm for the semiconductor wire growth. According to the VLS model, the cross section and crystallographic direction of the wires growth are controlled by the surface energies at the wire/gas phase (vacuum) and droplet/wire interfaces. One of the experimental observations consistent with this prediction is that the solid-liquid interface for a growing Si wire is a close-packed (111) plane.^{2,3} Therefore, Si wires will grow either vertically or inclined on the commercially available Si (100), (110), or (111) substrates,⁴ which complicates planar device fabrication and requires advanced processing techniques.^{5–9}

There have only been a few reports of lateral (parallel to substrate surface) Si wire growth.^{2,10,11} In contrast to the well-studied vertical growth mechanism,¹² the reasons for the lateral growth and the parameters controlling it remain relatively poorly understood due to the lack of experimental evidence. Isolating an individual parameter controlling the wire growth is complicated by the fact that the in-plane growth process involves three phases (vapour, liquid, and solid) and at least two interfaces (vapour-liquid and liquid-solid).¹²

Recently, our group reported reproducible growth of lateral Si wires (Si ridges) on the Si (100) substrates by molecular beam epitaxy (MBE).¹¹ The wires grow along two orthogonal $\langle 011 \rangle$ directions, with longer Si deposition time resulting in longer wires. In this paper, we present the experimental evidence showing the unique role of carbon at initial stages of growth. Once initiated, lateral growth can be controlled by tuning the temperature, size, and areal density of Au(Si) droplets, and the flux of incoming Si atoms.

Si wire growth was carried out in an ultrahigh vacuum MBE chamber (Kurt Lesker), containing Si (Alfa Aesar, 99.9999% purity) and Au (Canadian Mint, 99.999% purity) sources, both elements evaporated from water-cooled graphite crucibles using electron beam heating. The deposition rate was controlled using the quartz crystal monitors calibrated by independent Rutherford backscattering measurements. The substrates were heated by an electron beam

^{a)}Author to whom correspondence should be addressed. Electronic mail: sdedyuli@uwo.ca

heater (VG Ltd., Hastings) and their temperature was monitored by K-type thermocouples. A n-Si(100) wafer was covered with photoresist (Shipley 1827) to prevent small debris from spreading in the clean room environment and cut into $8 \times 10 \text{ mm}$ pieces. After removing the photoresist with acetone and isopropanol, these pieces were used as substrates for MBE depositions. Si substrates cut without using photoresist were also prepared as control samples.

Prior to loading the samples into the UHV MBE chamber, the native SiO₂ layer was removed by etching for 60 s in an HF buffer solution. Any SiO₂ that may have been formed during the transfer into UHV is then removed by outgassing at 600 °C for 15 min and subsequently heating the substrate at 850 °C for 10 min at 4×10^{-9} Torr base pressure prior to the deposition process. Next, a 1 nm thick gold film was deposited at room temperature at a growth rate of 4×10^{15} atoms cm⁻² min⁻¹ followed by annealing at 600 °C for 30 min in order to form catalytic gold-silicon alloy (Au(Si)) droplets of 90 nm diameter. The reported size of Au(Si) droplets correspond to the maximum of the size distribution. In the next step, Si was deposited at a rate of 2.3×10^{14} or 5×10^{14} atoms cm⁻² min⁻¹ for 15 to 360 min at 450, 550, and 650 °C and $\sim 1 \times 10^{-8}$ Torr pressure.

The samples were analyzed by scanning electron microscopy (LEO (Zeiss) 1530 SEM and LEO (Zeiss) 1540 XB FIB/SEM, NanoFab UWO) and medium energy ion scattering (MEIS) (95 keV H^+ beam, Tandetron Lab, UWO). The length of the wires were measured manually in ImageJ software.¹³

Typical SEM images of Si wires after 30 min and 240 min Si deposition are presented in Fig. 1. Here, the growth temperature was $650 \,^{\circ}$ C and silicon deposition rate was 5×10^{14} atoms cm⁻² min⁻¹. The lateral wire growth is only observed for silicon substrates previously covered with photoresist. On the control Si substrate (without photoresist), Si wires grow only around carbon-based contamination particles (Fig. 2(a)). We speculate that surface contamination originated from dust particles in the laboratory air deposited on the control substrate surface prior to loading it into UHV MBE chamber. After the removal of photoresist and subsequent thermal treatment, the Si (100) surface remains covered with carbon, as confirmed by *ex-situ* MEIS and energy dispersive X-ray (EDX) analysis carried out with the SEM microscope.



FIG. 1. SEM planar views of Si wires on Si (100) substrate after (a) 30 min and (b) 4 h of Si deposition. All scale bars: 1 nm.

MEIS shows that ≈ 5 ML of C (1 ML $\approx 6.8 \times 10^{14}$ at/cm² for Si (100)) need to be present on the surface to initiate Si wire growth. After Au deposition, carbon has a tendency to agglomerate in Au(Si) droplets as illustrated in EDX analysis images in Fig. 2(b), showing superposition of Au and C signals. This is not surprising if one takes into account the



FIG. 2. (a) SEM planar view of the Si wire growth initiated around Ccontaining contamination present (black arrow) on the control Si substrate. (b) EDX analysis of Au and C distribution in the highlighted area of electron image. All scale bars: 200 nm.

relatively high (up to 4.7 at. $\%^{14}$) solubility of carbon in liquid gold and extremely low (up to 9×10^{-4} at. $\%^{15}$) solubility of carbon in solid silicon. It should be noted that oxygen and carbon have long been recognized as the two major contaminants on wet etched Si surfaces,^{16,17} and carbon is the most difficult to remove by heating Si in ultrahigh vacuum.^{17,18}

In order to explain lateral wire growth, we start with one of the underlying assumptions in the VLS model, namely, that growth takes place under local thermodynamic equilibrium conditions close to the liquid-solid interface. The existence of local thermodynamic equilibrium implies that the growth of a silicon wire is determined by the minimization of the total Gibbs free energy; i.e., it is thermodynamically controlled. Next, we compare the main thermodynamic parameters controlling Si wire growth in the vertical and horizontal growth regimes.

Under fixed total pressure and temperature, the change in Gibbs free energy, δG^{Si} , for a vertical wire upon transfer of δN^{Si} silicon atoms from the gas phase to the crystal can be written as¹²

$$\delta G^{Si} = \delta N^{Si} (-\Delta \mu_{\infty}^{Si}) + \sum_{i} \delta A_{i}^{Si} \gamma_{i}^{Si}, \tag{1}$$

where the first term is due to increasing wire volume and the second term is due to increasing wire surface area. $\Delta \mu_{\infty}^{Si}$ denotes the change in chemical potential of Si atoms upon condensation from silicon vapour into bulk (infinite radius of curvature) silicon wire, δA_i^{Si} and γ_i^{Si} denote surface area and the specific free energy of the surface *i*, respectively. For vertical wires, it was shown¹⁹ that Si surface energy relationships combined with the minimization of surface-to-volume ratio can alone predict Si wire shapes and orientations.

For lateral silicon wires, the substrate surface diminishes with growth. Therefore, one has to consider the system including both the lateral wire and the underlying substrate when calculating the surface energy change during growth. As a result, the second term in Eq. (1) should be modified by including the corresponding surface energy of the substrate with a negative sign, $-\delta A_s^{Si} \gamma_s^{Si}$, in the sum.

In addition, we argue that the change in Gibbs free energy, δG^{Au} , for a Au(Si) droplet should also be taken into account for lateral growth

$$\delta G^{Au} = \delta N^C (-\Delta \mu_s^{Au}) + \sum_i \delta A_i^{Au} \gamma_i^{Au}, \qquad (2)$$

where the first term is the variation of the free energy of the system due to the dissolving of δN^C carbon atoms from the Si substrate into Au(Si) droplet, $\Delta \mu_s^{Au}$ represents the change in the chemical potential of the Au due to the formation of Au(C) liquid solution, and the second term is the decrease of the free energy of the gold droplet due to the dissolution of C. Overall, the minimization of δG^{Au} is responsible for initiating the lateral growth.

It is thermodynamically more favourable for a catalyst droplet to stay in contact with a carbon covered Si substrate (Fig. 3(a)). This way, the Au(Si) droplet lowers its chemical potential $\Delta \mu_s^{Au}$ and, possibly, the surface tension γ_i^{Au} by



FIG. 3. (a) Schematic of nucleation of a lateral Si wire: an Au(Si) droplet lowers its Gibbs free energy by consuming C impurities on the surface. (b) The stages of Si wire growth in MBE: 1—mass-transport in the gas phase; 2—surface diffusion; 3—incorporation into liquid droplet; 4—diffusion in the liquid phase; and 5—incorporation in the crystal lattice.

dissolving more carbon; in other words, it minimizes δG^{Au} . Additionally, lateral growth minimizes the fraction of the exposed Si (100) plane which is known to have larger surface energy density $\gamma_{(100)}^{Si}$ than the Si (111) plane.^{20–22} The observed preferential incorporation of C into Au(Si) droplets (Fig. 2(b)) and its high solubility in liquid gold¹⁴ both suggest that the chemical potential of a catalyst droplet is indeed reduced upon dissolving carbon impurities. We were not able to find any published data on the influence of carbon impurities on the surface tension of liquid gold. However, introducing surfactants, e.g., As and Sb, during thin film growth has been known to change the growth mode from island formation to layer-by-layer growth by lowering surface tensions of the growing materials.^{23,24}

While we have shown evidence supporting that nucleation of lateral Si wires is thermodynamically controlled, their subsequent growth is controlled kinetically as discussed further below. By analogy to the growth of thin films, the process that is thermodynamically controlled at the nucleation stage may be driven from equilibrium into a regime where kinetic parameters determine the film morphology. Temperature and pressure (flux) are typically used for that purpose.²⁵ The temperature of the substrate controls the diffusion and the desorption rates of adatoms, sticking coefficients, and surface energies. The pressure in the gas phase controls the impingement rate of adsorbing atoms. In our MBE system, the temperature of the substrate and deposition (impingement) rate of silicon atoms can be controlled independently. This offers a unique playground for testing various hypotheses regarding the wire growth mechanism and thereof developing growth recipes for possible applications.

A schematic of lateral wire growth process is shown in Fig. 3(b). Five principal steps can be distinguished: (1) masstransport in the gas phase; (2) surface diffusion; (3) preferential incorporation of atoms into liquid droplets; (4) diffusion in the liquid phase; and (5) precipitation of Si into a growing wire. Here, we have adopted four growth steps (1, 3, 4, and 5) characteristic to vertical wire growth by CVD¹² and added a surface diffusion step (2) specific to MBE wire growth.²⁶ Several of these stages (1, 2, and 3) can be a ratedetermining step for the formation of the silicon wire array. For example, we have shown previously¹¹ that increasing the gold coverage will make step 3 a rate-determining one. In that case, higher areal density and smaller relative size of catalyst droplets lead to the formation of the multiple small silicon islands. Growth and coarsening of those islands caused a rough, multilayer Si film to grow.

The mass-transport regime (step 1) will be a rate limiting step at relatively high growth temperatures T and low fluxes of silicon atoms F. In this regime, all silicon atoms landing on the substrate will have enough time to reach a Au(Si) droplet by surface diffusion and precipitate into a growing Si wire. Under these conditions, the steady state solution to the diffusion equation for Si adatoms on Si (100) surface (see supplementary material²⁷) predicts that the length of a lateral Si wire will be directly proportional to the Si deposition time, t, and incoming Si flux, F,

$$L = c(r_{Au}, \lambda_s)Ft, \qquad (3)$$

where $c(r_{Au}, \lambda_s)$ is a constant factor that depends on the radius of the gold droplet r_{Au} and diffusion length λ_s of Si adatoms. To confirm this, we measured the average length of Si wires at $T = 650 \,^{\circ}$ C and $F = 5 \times 10^{14}$ atoms cm⁻² min⁻¹ for different Si deposition times (Fig. 4). In agreement with theoretical predictions, we found linear growth for short Si deposition times (t < 3 h). Deviation from linear growth at longer Si deposition times are caused by a decrease in the Si flux F over time, as confirmed by *in situ* measurements with crystal quartz monitor.²⁸

In MBE, the silicon atoms are thermally evaporated and typically have low kinetic energies ($k_BT \sim 0.1 \text{ eV}$) when they arrive at the surface.²⁹ Low energy deposition conditions imply that atoms attach at the sites very near to the impingement point of the atom with the surface unless they are thermally activated on the surface. If the deposition rate *F* is high, or the substrate's temperature *T* is low, the atoms are unable to diffuse to catalyst droplets nearby and they nucleate a new island instead. The growth of individual Si islands is thus competing with the incorporation of Si atoms into Au(Si) droplets, and, as a result, a rough Si film develops.

In Fig. 5, we show how the diffusion regime (step 2) can be activated by lowering the growth temperature to 450 °C



FIG. 4. The length of lateral Si wires as a function of Si deposition time. Constant growth rate, L = Ct, is also shown for comparison.



FIG. 5. SEM micrograph of a diffusion limited growth of Si wires. The growth temperature was T = 450 °C and flux $F = 5 \times 10^{14}$ atoms cm⁻² min⁻¹. Scale bar: 100 nm.

and keeping the flux the same, $F = 5 \times 10^{14}$ atoms cm⁻² min⁻¹. In this case, the surface diffusion coefficient, $D = D_0 \exp(-E_a/k_BT)$, is lower by a factor of 2 (for a diffusion barrier $E_a = 0.6$ eV (Ref. 30)), so that adatoms tend to stay where they have landed, nucleating multiple silicon islands. When a slow-moving gold droplet encounters one of these islands, the island blocks its path. The silicon wire can then either turn or cease growing. Minimizing the island density will thus decrease the number of turned or terminated wires.

The island density N should decrease with a decrease of flux F and/or increase of diffusion coefficient D (or temperature T) and has the qualitative form $N \sim F^p/D^q$.³¹ The values of p and q are positive and are dependent on the nucleation and growth mechanisms. It is then possible to compensate the low temperature effects by decreasing the flux of Si atoms. Indeed, we were able to grow Si wires at 450 °C by lowering the Si flux, $F = 2.3 \times 10^{14}$ atoms cm⁻² min⁻¹ (see supplementary material²⁷). However, lower growth rate and incomplete suppression of island formation render such growth conditions impractical.

In summary, we have presented thermodynamic arguments proving that carbon on the level of ≈ 5 ML initiate the lateral growth of silicon wires on the Si (100) substrate. Controlled deposition of a carbon layer after the substrate's cleaning stage can thus be used to initiate the lateral growth of semiconductor wires which otherwise grow vertically.

Upon nucleation, Si wire growth is controlled kinetically by the following three parameters: the flux of incoming silicon atoms (mass-transport regime), the surface diffusion of Si adatoms (the diffusion regime), or the areal density of Au(Si) droplets (the Au-incorporation-limited regime). Among these three regimes, the mass-transport regime, realized at high deposition temperatures ($T \ge 650 \,^{\circ}$ C), low Si fluxes ($F \le 5 \times 10^{14}$ atoms cm⁻² min⁻¹), and large interwire separation ($\Delta r_{avg} > \lambda_s$), is beneficial for future applications. In this regime, the wires grow linearly with time, provided the temperature and flux are kept constant. This fact can be used to produce interconnections between two metal electrodes deposited on the surface similar to growth of silicon logic gates reported by Kim *et al.*⁸ Adding precise positioning of catalyst droplets and using miscut substrates with atomic steps to guide the wire growth can further result in self-assembled wire arrays of desired complexity.

The authors gratefully acknowledge the financial support from NSERC and the University of Western Ontario in pursuing this research. The authors acknowledge the Nanofabrication facility (UWO) for SEM/EDX measurements. S.D. would like to thanks Gabe Keenleyside for help with statistical analysis of SEM images and Jack Hendriks (Tandetron Lab, UWO) for assistance with the MBE chamber.

- ¹R. S. Wagner and W. C. Ellis, Appl. Phys. Lett. 4, 89 (1964).
- ²R. S. Wagner and W. C. Ellis, Trans. Metall. Soc. AIME **233**, 1053 (1965).
- ³Y. Wu, Y. Cui, L. Huynh, C. J. Barrelet, D. C. Bell, and C. M. Lieber, Nano Lett. 4, 433 (2004).
- ⁴S. A. Fortuna and X. Li, Semicond. Sci. Technol. 25, 024005 (2010).
- ⁵Y. Cui and C. M. Lieber, Science **291**, 851 (2001).
- ⁶R. He, D. Gao, R. Fan, A. I. Hochbaum, C. Carraro, R. Maboudian, and P. Yang, Adv. Mater. **17**, 2098 (2005).
- ⁷M. S. Islam, S. Sharma, T. I. Kamins, and R. S. Williams, Nanotechnology **15**, L5 (2004).
- ⁸D. R. Kim, C. H. Lee, and X. Zheng, Nano Lett. 10, 1050 (2010).
- ⁹N. J. Quitoriano, W. Wu, and T. I. Kamins, Nanotechnology **20**, 145303 (2009).
- ¹⁰S. J. Rathi, D. J. Smith, and J. Drucker, Nano Lett. **13**, 3878 (2013).
- ¹¹S. N. Dedyulin, G. Fanchini, and L. V. Goncharova, Cryst. Growth Des. **14**, 1193 (2014).
- ¹²E. I. Givargizov, *Highly Anisotropic Crystals*, 1st ed. (D. Reidel Publishing Co., Boston, 1987).
- ¹³C. A. Schneider, W. S. Rasband, and K. W. Eliceiri, Nat. Methods 9, 671 (2012).
- ¹⁴H. Okamoto and T. B. Massalski, Bull. Alloy Phase Diagrams 5, 378 (1984).
- ¹⁵F. Durand and J. C. Duby, J. Phase Equilib. 20, 61 (1999).
- ¹⁶B. R. Weinberger, G. G. Peterson, T. C. Eschrich, and H. A. Krasinski, J. Appl. Phys. **60**, 3232 (1986).
- ¹⁷R. C. Henderson, J. Electrochem. Soc. **119**, 772 (1972).
- ¹⁸R. C. Henderson, R. B. Marcus, and W. J. Polito, J. Appl. Phys. 42, 1208 (1971).
- ¹⁹V. Schmidt, J. V. Wittemann, and U. Gösele, Chem. Rev. **110**, 361 (2010).
- ²⁰D. Eaglesham, A. White, L. Feldman, N. Moriya, and D. Jacobson, Phys. Rev. Lett. **70**, 1643 (1993).
- ²¹D. M. Follstaedt, Appl. Phys. Lett. 62, 1116 (1993).
- ²²A. Stekolnikov, J. Furthmüller, and F. Bechstedt, Phys. Rev. B 65, 115318 (2002).
- ²³M. Copel, M. C. Reuter, E. Kaxiras, and R. M. Tromp, Phys. Rev. Lett. 63, 632 (1989).
- ²⁴M. Horn von Hoegen, F. K. LeGoues, M. Copel, M. C. Reuter, and R. M. Tromp, Phys. Rev. Lett. **67**, 1130 (1991).
- ²⁵K. W. Kolasinski, Surface Science: Foundations of Catalysis and Nanoscience, 2nd ed. (John Wiley & Sons Ltd., Mississauga, ON, Canada, 2008), pp. 345–351.
- ²⁶P. Werner, N. D. Zakharov, G. Gerth, L. Schubert, and U. Gosele, Int. J. Mater. Res. **97**, 1008 (2006).
- ²⁷See supplementary material at http://dx.doi.org/10.1063/1.4869444 for the analytical solution of the diffusion equation with respect to in-plane Si wire growth and for the images of lateral Si wires grown at low temperature and flux conditions.
- ²⁸Decreasing of the Si flux over time may be caused by geometric shadowing from the edges of the hole formed on the surface of silicon source during evaporation.
- ²⁹H. N. G. Wadley, X. Zhou, R. A. Johnson, and M. Neurock, Prog. Mater. Sci. 46, 329 (2001).
- ³⁰We have used a lowest reported value for $E_a = 0.6$ eV calculated by G. Brocks *et al.*, Phys. Rev. Lett. **66**, 1729 (1991) for diffusion of Si adatoms along the dimer rows on Si (100) surface.
- ³¹Z. Zhang and M. G. Lagally, Science **276**, 377 (1997).