

PHYSICS 359E

DIGITAL LOGIC GATES AND PULSE MEASURING CIRCUITS

I. DIGITAL LOGIC GATES

Introduction:

All digital computers are based on the binary number system, i.e., a system in which a digit can have only one of two values, a '0' or a '1'. These numbers can represent the state of a simple switch: switch closed, or ON=1; switch open, or OFF=0. All operations of the computer can then be described in terms of binary numbers, or equivalently by the state of suitable combinations of on-off electronic switches. These combinations are known as logic gates and they control the flow of binary information (in the form of pulses). All binary logic operations (in any computer) can be realized by combinations of only three basic operations or logic gates. These are known as AND, OR, NOT.

As an illustration of the ideas involved, consider the AND gate. The operation of this gate is analogous to that of a circuit containing two switches in series as shown below. Let us describe the state of each switch A and B by a number which will be 1 if the switch is closed and 0 if the switch is open. The state of the point F can also be describe by a number which we take to be 0 if the voltage at F is 0 and 1 if the voltage is equal to the battery voltage V_b . The possible states this circuit can be described by a truth table which lists the state of F corresponding to all possible states of A and B. This is given below.

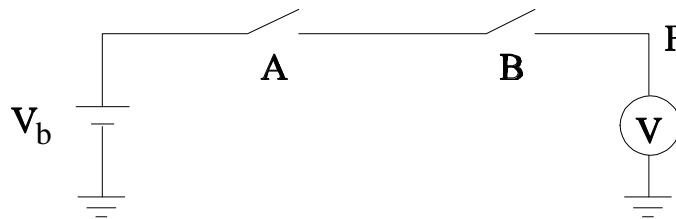


Fig. 1. Representation of an AND logic gate.

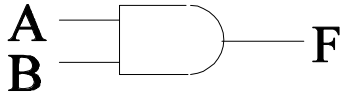
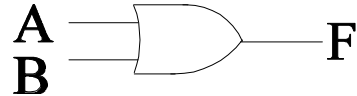
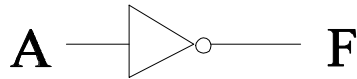
Truth Table for AND gate

State of A	State of B	State of F
0 (open)	0 (open)	0 ($V = 0$)
0	1 (closed)	0
1	0	0
1	1	1 ($V = V_b$)

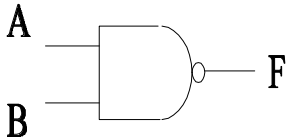
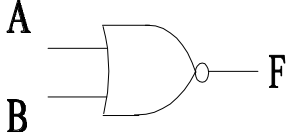
This may seem very trivial, but it illustrates the basic ideas involved in analyzing digital logic circuits. In general, a truth table lists the output state of the circuit corresponding to each possible combination of

input states.

The table below contains the symbols and truth tables for the three basic logic gates.

TYPE	SYMBOL	TRUTH TABLE															
AND		<table><thead><tr><th>A</th><th>B</th><th>F = A.B</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>0</td></tr><tr><td>1</td><td>0</td><td>0</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table>	A	B	F = A.B	0	0	0	0	1	0	1	0	0	1	1	1
A	B	F = A.B															
0	0	0															
0	1	0															
1	0	0															
1	1	1															
OR		<table><thead><tr><th>A</th><th>B</th><th>F = A+B</th></tr></thead><tbody><tr><td>0</td><td>0</td><td>0</td></tr><tr><td>0</td><td>1</td><td>1</td></tr><tr><td>1</td><td>0</td><td>1</td></tr><tr><td>1</td><td>1</td><td>1</td></tr></tbody></table>	A	B	F = A+B	0	0	0	0	1	1	1	0	1	1	1	1
A	B	F = A+B															
0	0	0															
0	1	1															
1	0	1															
1	1	1															
NOT		<table><thead><tr><th>A</th><th>F = A</th></tr></thead><tbody><tr><td>0</td><td>1</td></tr><tr><td>1</td><td>0</td></tr></tbody></table>	A	F = A	0	1	1	0									
A	F = A																
0	1																
1	0																

Two other frequently used logic gates are the NAND and the NOR gates. Their symbols and truth tables are shown below. It is clear that these gates are equivalent to the AND and OR gates followed by a NOT gate.

TYPE	SYMBOL	TRUTH TABLE															
NAND		<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>$F=A.B$</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>1</td> </tr> <tr> <td>1</td> <td>0</td> <td>1</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	$F=A.B$	0	0	1	0	1	1	1	0	1	1	1	0
A	B	$F=A.B$															
0	0	1															
0	1	1															
1	0	1															
1	1	0															
NOR		<table border="1"> <thead> <tr> <th>A</th> <th>B</th> <th>$F=A+B$</th> </tr> </thead> <tbody> <tr> <td>0</td> <td>0</td> <td>1</td> </tr> <tr> <td>0</td> <td>1</td> <td>0</td> </tr> <tr> <td>1</td> <td>0</td> <td>0</td> </tr> <tr> <td>1</td> <td>1</td> <td>0</td> </tr> </tbody> </table>	A	B	$F=A+B$	0	0	1	0	1	0	1	0	0	1	1	0
A	B	$F=A+B$															
0	0	1															
0	1	0															
1	0	0															
1	1	0															

For reasons of convenience in manufacture, the NAND gate is the most commonly used type of gate. In the lab exercises, we will start with the integrated circuit 7400, which contains four NAND gates in a single chip. Each gate has two inputs A and B and performs the operation $F = A.B$, i.e. the output is zero if and only if A and B are both one. While it is convenient to consider the OR, NOT, and NOR gates as separate elements, in fact these gates can easily be constructed by suitable circuits involving only the NAND gate.

Note that the number of gate inputs is not limited to two. The IC 7420 contains two four-input NAND gates. Each gate performs the operation $F = A.B.C.D$, i.e. the output is zero if and only if all of A, B, C and D are one. Of course, such a four-input gate could also be constructed using a combination of two-input gates.

PROCEDURE:

All the logic gates used in the exercises below are known as TTL (transistor-to-transistor) logic. These have the convenient property that the output of any gate can be used directly as input to another gate. All these TTL circuits are operated from a 5 V power supply, and the binary digits 0 and 1 are represented by low and high voltages on the gate terminals. A data sheet for the 7400 integrated circuit (IC) is given in the Appendix, and shows that LOW (0) is a voltage in the range 0 - 0.4 V and HIGH (1) is a voltage in the range 2.4 - 5.0 V.

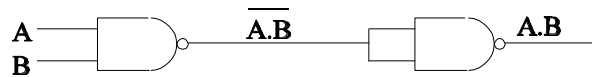
Measurements are carried out using the test boxes provided. They contain the necessary power supply, a pulser, and an LED (light-emitting diode) display for observing the state of any point in a circuit. They also have a very flexible system of socket pins for mounting the IC and making the necessary interconnections.

1. Basic observations:

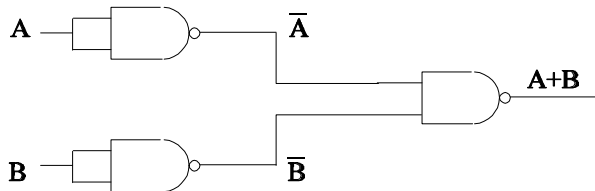
Using the 7400 IC, do the following:

- a) Using the LED display as a probe, confirm the NAND gate truth table.

b) Construct an AND gate and check the truth table.



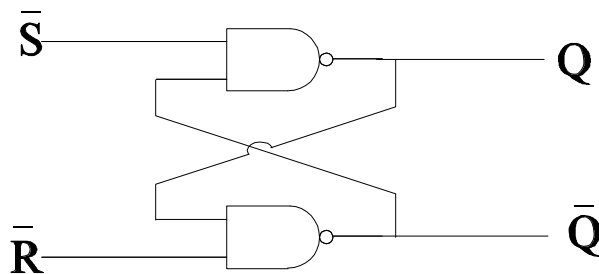
c) Construct an OR gate and check the truth table.



d) Change the above OR gate to a NOR by adding one more NAND gate and check the truth table.

2. Flip-flops: Memory and Counting Devices

To store binary information we require a device which has two distinct states and will remain in one state until instructed to change. One such device is the bistable multivibrator or flip-flop. A simple flip-flop may be constructed from two NAND gates as follows:



This is known as an R S flip-flop, the S and R standing for Set and Reset.

To understand the operation of this circuit, consider one stable state in which $R = S = Q = 1$ and $Q = 0$. If we now make $S = 0$, the output will change state (flip) to give $Q = 1, Q = 0$. If we now return S to state $S = 1$, the state of Q and Q will remain unchanged. Finally if we make $R = 0$, the circuit will return to its original state (flop) to give $Q = 1, Q = 0$.

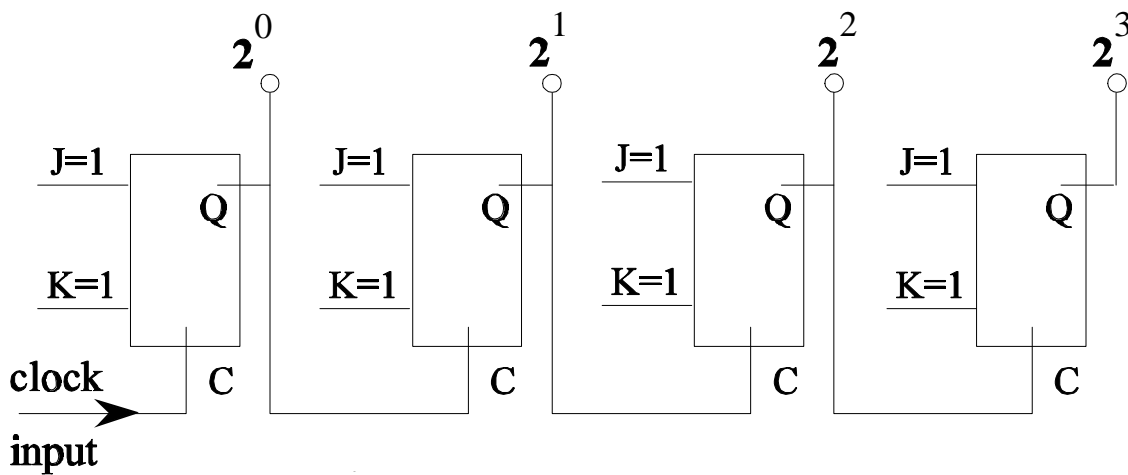
a) Wire up the R S flip-flop and construct a truth table showing the Q and Q logic states both before and after applying various logic states to the R and S inputs.

A more versatile flip-flop is the 'clocked' JK flip-flop. Such a device can in principle be constructed from NAND gates, but is normally packaged as an integrated circuit such as the 7473, for which the specifications are given in the Appendix.

With this device the JK inputs correspond to the SR inputs of the simple multivibrator. In addition there is a CLEAR input and a CLOCK input. Changes in the state of the outputs Q and \bar{Q} occur only after a clock pulse is supplied. The clock pulse goes from LOW to HIGH, then back to LOW in a short time; it is on the HIGH-to-LOW transition that the actual state change occurs. The state of output Q after the occurrence of a clock pulse is given by the truth table on the spec. sheet. Note that a LOW input to CLEAR sets Q to LOW independent of J,K, and CLOCK inputs.

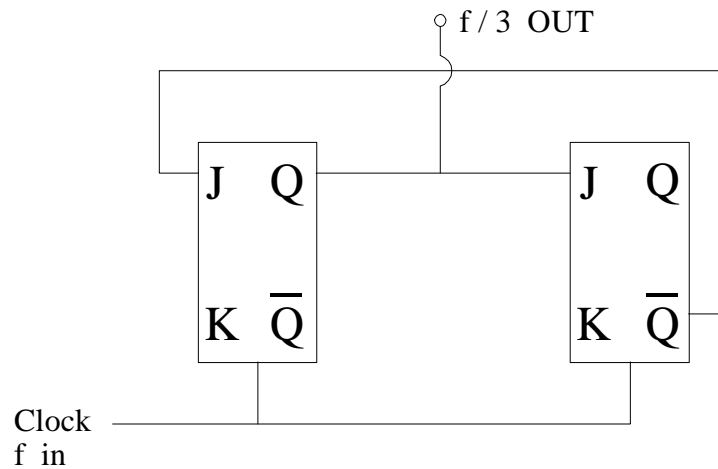
b). Using a 7473 and applying single pulses to the clock input, verify the truth table as given in the data sheet.

c) A common use of JK flip flops is for counters. Wire up the following simple binary counter which will count incoming pulses to the clock input and register the total count on the Q outputs. The CLEAR input Rd1 (not shown) on each 7473 chip must be connected to HIGH.



d) Another function of flip-flops used as counters is as frequency dividers. The circuit above can be used as a simple divide by 2, 4, 8 or 16 frequency divider. Put a 1 kHz clock signal into the input of the above circuit and observe the input and each of the outputs on the 2 channels of your oscilloscope.

e) The above counter is known as a ripple counter. Another type, in which the clock pulses are applied simultaneously to each flip-flop is known as a synchronous counter. Construct the synchronous counter below which divides by 3. Construct a truth table for the circuit to verify that it does operate as claimed, and graph the input and output waveforms.



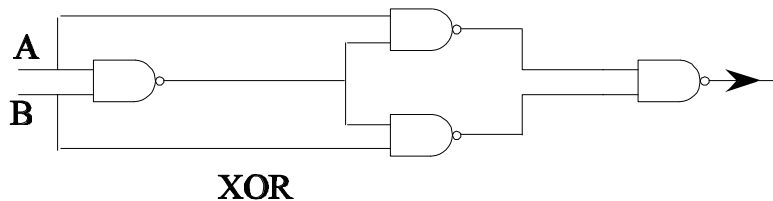
II: Pulse measuring circuits:

Logic circuits can be used to form some standard laboratory circuits used to process and analyze information received in the form of discrete pulses. This is the usual signal provided by particle counters such as scintillation detectors, photomultipliers, channeltrons, etc. It is common to convert other types of signal to pulse form so that they can be processed by digital logic circuitry. Some of the more common circuits are as follows:

a) Coincidence gate

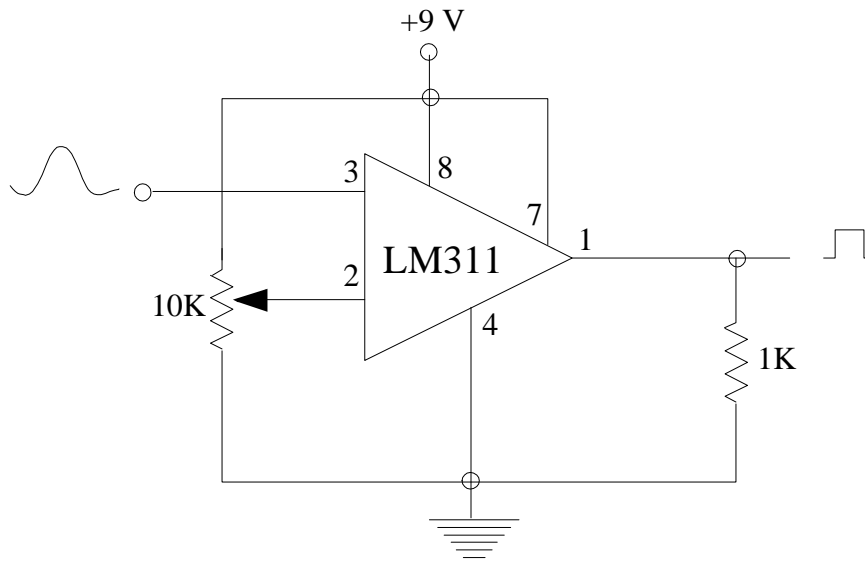
A simple AND or NAND gate can serve as a coincidence circuit. Such a circuit produces an output signal if and only if pulses are received by both inputs simultaneously.

b) Anticoincidence gate



In digital terminology, this is an EXCLUSIVE OR gate. It produces an output pulse if one input terminal receives a pulse but no output if both inputs receive simultaneous pulses. An EXCLUSIVE OR gate constructed from NAND gates is shown below. The actual gates are provided in the 7400 QUAD 2-input integrated circuit (see Appendix). Assemble the circuit as shown and determine its truth table.

c) Comparator

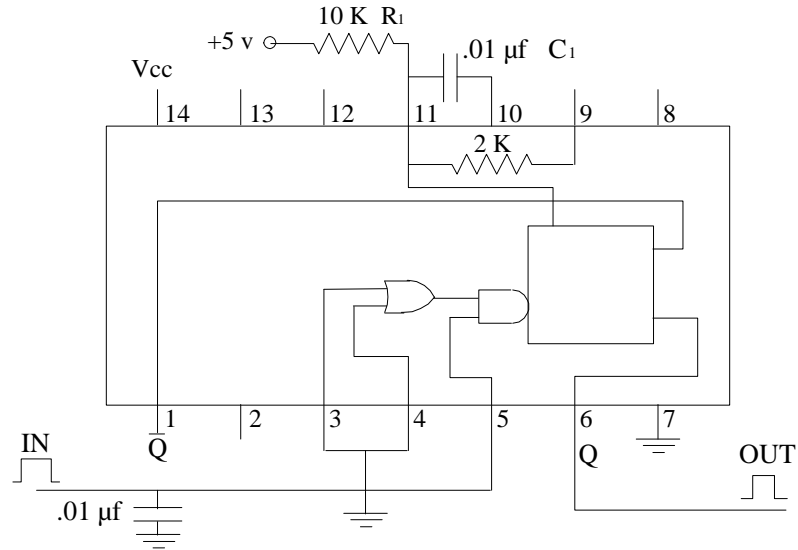


The comparator is a circuit that is partly analog but has a logical function. Its function is to compare two inputs (signal and reference) and output a high or low depending on which is larger. Connect the circuit as shown and observe the output for a sine and a square wave input of various voltages at a few hundred Hz. The reference input is provided by the $10\text{K}\Omega$ potentiometer connected between ground and 9 V.

For simplicity, we are using only a positive power supply (9 V battery) rather than a bipolar (\pm) power supply. Because of this, you will get an inappropriate output for a negative input. Use your oscilloscope to monitor the input and keep it between 0 and 9 V. Display both the input and output on your oscilloscope and observe the effect on the output pulse width as you vary the signal or reference amplitude.

For this section and the rest of this experiment, your report should include a sketch of the waveforms with timing and amplitude information indicated.

d) Monostable multivibrator



Pulses of varying widths can be awkward to deal with in a digital counting or timing circuit, so a monostable multivibrator (also called a "one-shot") is used to produce a constant-width pulse. The output pulse may be triggered by either the rising or falling edge of the input pulse. Connect the output of your comparator circuit to the input of the one-shot circuit (74121) shown below and observe the output of the one-shot as you again vary the signal amplitude. The pulse width of the output of the one-shot is determined by the time constant of the RC circuit formed by R1 and C1. Leave C1 at 0.01μf and observe the effect of varying R1. You may use a decade resistance box for R1 if one is available.

e) Single Channel Analyzer

Explain how the addition of another comparator set to a different voltage, and an EXCLUSIVE OR gate can be used to produce an output pulse only if the input is between two levels. Such a device is known as a single channel analyser, a name which makes sense in the context of what a multichannel analyser (MCA) does. Sketch out such a circuit in your report.